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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,795	05/01/2001	Jack H. Linn	87552.055101/SE-1472TD.A	7145

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EXAMINER

SARKAR, ASOK K

ART UNIT PAPER NUMBER

2829

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/846,795

Applicant(s)

LINN ET AL.

Examiner

Asok K. Sarkar

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 24-44 and 46-48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 24-44 and 46-48 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Reply to Appeal Brief*

1. In response to Applicant's Appeal Brief, Examiner has carefully reviewed the record and discovered that the 103 rejections of claims 30, 32 – 34, 39 and 42 – 44 would benefit from further elaboration in the interest of customer service. The prosecution of the case is hereby reopened to clarify those rejections.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 24 – 29, 31, 35 – 38, 40, 41 and 46 - 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Henley, US 6,083,324.

Regarding claims 24, 26, 28, 29, 36, 38, 40 and 46, Henley teaches a bonded SOI substrate comprising all the structural elements of these claims as follows:

- a wafer comprising a first layer of monocrystalline Si material adjacent first surface of the wafer with reference to Fig. 8;

- a planar intrinsic gettering layer 808 with reference to Fig. 8 within Si inherently containing silicon ions. Henley teaches gettering zone of substantially pure semiconductor material in column 3, lines 3 – 8;
- an insulating bond layer 809 with reference to Fig. 8;
- a handle wafer 811 with reference to Fig. 8;
- semiconductor device 801 – 803 on the second layer with reference to Fig. 8 or the epitaxial layer 18 with reference to Fig. 1D.

These claims are product by process claims and are subject to the following:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

In the instant case, Henley teaches a semiconductor device, having planar gettering zone similar to that of the Applicant. The Henley's device is indistinguishable from that of the Applicant since the heating step in forming Henley's device will restore the damage caused by the implantation converting it to undamaged monocrystalline semiconductor material (see column 5, lines 4 – 14).

Regarding claims 25, 27, 37 Henley teaches device is a FET in column 8, line 33.

Regarding claims 31 and 41, Henley teaches handle wafer 414 with reference to Fig 4 of silicon and bonding layer of silicon dioxide (see column 6, lines 43 - 44).

Regarding claims 35, 47 and 48, Henley teaches two or more semiconductor devices 801 – 803, which are laterally isolated by regions 804 with reference to Fig. 8 in column 8, lines 31 – 48.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 30 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley, US 6,083,324 in view of Hori, US 5,731,637.

Henley fails to expressly teach implantation with Si.

Hori teaches forming gettering layers by implanting Si in column 3, lines 43 – 45.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Henley by forming gettering layer with Si implantation since the intrinsic gettering layers can be formed by implanting Si as taught by Hori.

Moreover, the claims relate to a product and as was described earlier, it is immaterial how the gettering layer is made and therefore the device claimed in the instant case is identical to that of Henley's. Note that a "product by process" claim is directed to the product per se, no matter how actually made,

6. Claims 32 - 34 and 42 - 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley, US 6,083,324 in view of Horikawa, US 6,046,095.

Henley teaches the thickness of the first layer to be between 0.1 – 0.8 micron in column 4, line 21. He also teaches that the thickness of the gettering layer and consequently the remaining second layer on the starting wafer will depend on various

factors especially the energy in various places in columns 4 – 6, but fails teach the thickness of the second monocrystalline semiconductor layers and the gettering zone.

Horikawa teaches the relationship for evaluation of the gettering efficiency for the silicon wafer with the thickness of the gettering layer in column 3, lines 30 - 50

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control these parameters during the formation of the SOI substrate as taught by Henley and Horikawa through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller*, *Lacey and Hall* (10 USPQ 233 – 237).

### ***Response to Arguments***

7. Applicant's comments/arguments in the Appeal Brief are moot in view of the reopening of the prosecution. Nevertheless, the Examiner provides the following relevant points of Applicant's arguments to ensure that the Applicant clearly understands the Examiner's position. Regarding the independent claims 24, 26, 28 and 38, the Applicant argues that Henley reference does not teach forming a semiconductor device of undamaged monocrystalline semiconductor material. The instant invention

claims a product (semiconductor device) and therefore should be compared to the product taught by the reference. As is pointed out in the rejection, the product taught by Henley is indistinguishable from the present invention since the heating step in forming Henley's device will heal the implantation damage in Henley's device and restore it to the original undamaged condition as claimed by the instant invention. Since Henley's device has an annealed layer, the original electrical characteristics will be restored by the annealing process and the same layer will be indistinguishable from the Applicant's undamaged monocrystalline silicon layer.

The Applicant's argument regarding the dependent claims is moot in view of the new ground of rejection. The process of making a device receives weight for a device claim to the degree that it defines the structure.

### ***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 308 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703 308 1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Application/Control Number: 09/846,795  
Art Unit: 2829

Page 7

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar  
May 23, 2008

A handwritten signature in black ink, appearing to read 'KAMAND CUNEO', with a large loop at the end.

KAMAND CUNEO  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800